What is Claimed Is:

1. A semiconductor memory device, comprising:

a memory cell array;

a data buffer for processing data read from or written to the memory cell array; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal.

2. The device of claim 1, wherein the data width control circuit comprises:

a decoder for decoding the external address signal in response to a data access command to generate a first control signal; and

a data buffer controller, responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer.

3. The device of claim 1, wherein the data width control circuit selectively controls the data width of the data buffer by generating a control signal that masks or unmasks one or more bits of the data buffer.

4. The device of claim 3, wherein a masked bit is prevented from being input to the memory cell array from the data buffer.

5. The device of claim 3, wherein a masked bit is prevented from being output from the data buffer.

6. The device of claim 1, wherein the data buffer has a width of *n* bits and wherein the data width of the data buffer is selectively controlled to be *n* bits or less.

7. The device of claim 2, wherein the decoder comprises:

a switching circuit; and

a logic circuit, wherein the switching circuit is response to the data access command to pass the external address signal to the logic circuit and wherein the logic circuit processes the external command to generate the first control signal based on the external command.

8. The device of claim 7, wherein the logic circuit comprises a plurality of parallel connected AND gates that receive the external address signal, and wherein the first control signal comprises a plural bit signal comprised of the output signals from the AND gates.

9. The device of claim 8, wherein the data buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the data access command, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprise a plural bit signal comprised of the output signals of the switches.

10. A semiconductor memory device, comprising:

a memory cell array;

a data output buffer for outputting data read from the memory cell array;

a data input data buffer for inputting data to be written to the memory cell array; and

a data width control circuit for selectively controlling a data width of the data output buffer or the data input buffer in response to an external address signal.

11. The device of claim 10, wherein the data width control circuit comprises:

a decoder which is activated in response to a read command signal or write command signal to decode the external address to generate a first control signal;

a data input buffer controller which is activated in response to the write command

signal to generate a second control signal for controlling the data width of the data input buffer based on the first control signal; and

a data output buffer controller which is activated in response to the read command signal to generate a second control signal for controlling the data width of the data output buffer based on the first control signal.

12. The device of claim 10, wherein the data width control circuit selectively controls the data width of the data input buffer or data output buffer by generating a control signal that masks or unmasks one or more bits of the data buffer.

13. The device of claim 12, wherein a masked bit is prevented from being input to the memory cell array from the data input data buffer.

14. The device of claim 12, wherein a masked bit is prevented from being output from the data output buffer.

15. The device of claim 10, wherein the data input and output buffers have a width of *n* bits and wherein the data width of the data buffers are selectively controlled to be *n* bits or less.

16. The device of claim 11, wherein the decoder comprises:

a switching circuit; and

a logic circuit, wherein the switching circuit is response to the read or write command signal to pass the external address signal to the logic circuit and wherein the logic circuit processes the external command to generate the first control signal based on the external command.

17. The device of claim 16, wherein the logic circuit comprises a plurality of parallel connected AND gates that receive the external address signal, and wherein the first control signal comprises a plural bit signal comprised of the output signals from the AND gates.

18. The device of claim 17, wherein the data input buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the write command signal, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprising a plural bit signal comprised of the output signals of the switches.

19. The device of claim 17, wherein the data output buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the read command signal, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprising a plural bit signal comprised of the output signals of the switches.

20. An integrated circuit device, comprising:

a data buffer; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal.

21. A memory system, comprising:

a controller for generating data access command signals and address signals; and

a semiconductor memory device comprising:

a memory cell array;

a data buffer for processing data read from or written to the memory cell array; and

a data width control circuit for selectively controlling a data width of the

data buffer in response to an external address signal.

22. The system of claim 21, wherein the controller is a microprocessor unit.

23. The system of claim 21, wherein the controller is a network control unit.

24. The system of claim 21, wherein the controller is a memory controller.

25. A method for providing data I/O (input/output) width control in a semiconductor memory device, comprising the steps of:

generating a data width control signal in response to an external address signal; and

controlling a data width of a data buffer in response to the data width control signal.

26. A semiconductor memory device, comprising:

a memory cell array;

a data buffer for processing data read from or written to the memory cell array by a read command or write command; and

a data width control circuit for selectively controlling a data width of the data

buffer in response to an external address signal accompanied with the read command or write command.

27. A semiconductor memory device, comprising:

a memory cell array;

a data buffer for processing data read from or written to the memory cell array by a read command or write command; and

a data width control circuit for selectively controlling a data width of the data buffer in response to a redundant external address signal accompanied with the read command or write command.